IN THE CLAIMS:

Please cancel claims 1-33 without prejudice or disclaimer of the subject matter recited therein. Please amend the claims as follows (all claims listed):

Claims 1.-33. (Cancelled)

34. (New) A method of pausing processing of instructions, comprising:

determining whether a first instruction for a first thread is an instruction of a first type at a pipeline stage of a processor;

pausing processing of instructions of said first thread at said pipeline stage for a period of time if said first instruction is of a first type while processing instructions from a second thread; and

resuming processing of instruction of said first thread responsive to said first instruction at said pipeline stage.

35. (New) The method of claim 34 further comprising decoding said first instruction into a first microinstruction and a second microinstruction.

36. (New) The method of claim 35 wherein said first microinstruction causes a value to be stored in memory for said first thread.

37. (New) The method of claim 36 further comprising:

processing said microinstruction for execution when said value stored in memory is reset.

38. (New) The method of claim 37 wherein said value stored in memory is reset when said first microinstruction is retired.

39. (New) A method comprising:

determining whether a first instruction of a first thread is an instruction of a first type;

initiating a counter; and

pausing processing of instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value while processing instructions for a second thread.

40. (New) The method of claim 39 wherein said first instruction includes an operand and said initiating includes loading said counter with said operand.

41. (New) The method of claim 40 further comprising resuming processing instructions of said first thread after said counter reaches said predetermined value.

42. (New) An apparatus, comprising:

a decode unit to determine whether a first instruction of a first thread is an instruction of a first type, said decode unit to pause processing of instructions of said first thread at a pipeline stage of a processor for a period of time while instructions from a second thread can be processed, said decode unit further to cause resumption of processing instructions of said first thread in response to said first instruction.

43. (New) The apparatus of claim 42 wherein said first instruction comprises a first microinstruction and a second microinstruction.

44. (New) The apparatus of claim 43 further comprising:

a memory, wherein said first microinstruction causes a value to be stored in memory for said first thread.

45. (New) The apparatus of claim 44 wherein said decode unit processes said second microinstruction when said value stored in memory is reset.

46. (New) The apparatus of claim 45 further comprising:

a retire unit coupled to said decode unit wherein said retire unit causes said value stored in memory to be reset when said first microinstruction is retired by said retire unit.

47. (New) An apparatus comprising:

a decode unit to determine whether a first instruction for a first thread is an instruction of a first type;

a counter coupled to said decode unit, said counter to be initiated if said first instruction for said first thread is an instruction of said first type, said decode unit to pause processing instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value; and

wherein instructions for a second thread can be processed while instructions of said first thread are paused from being processed and wherein said decode unit resumes processing instructions of said first thread in response to said first instruction.

48. (New) The apparatus of claim 47 wherein said first instruction includes an operand to be loaded into said counter.

49. (New) The apparatus of claim 48 wherein said decode unit can continue to operate while said first thread is paused from being processed.